PerfectVIPs
Right Tools... Perfect Chip

PCI EXPRESS 2.0 VIP

GENIE-PCIe2™

PCI EXPRESS 2.0 VERIFICATION IP

OVERVIEW

The Genie-PCIe2™ Verification IP Products provide the most robust verification solution for PCIe 2.0 based designs. The intelligent **Verification Engine**, advanced **Interface Inspector** and comprehensive **Compliance Suite** provide the Perfect combination of tools to reduce design risk, verification time and project costs. Genie-PCIe™

The **Genie-PCIe2™ VIP** provides a quick and efficient way to verify any PCIe based design – Root Complex, End Point or Switch. It supports the PCIe 2.0 specification and is backwards compatible with PCIe 1.1 and 1.0a specification addressing all layers of the PCIe protocol – Phy, Datalink, Transaction layer and Configuration Space. Genie-PCIe provides a complete verification solution that includes multi-language support and OVM methodology.

The Genie-PCIe VIP provides:

- Bus Functional Models
- Directed and Random Transaction Generator
- Packet & Order set Generator
- Error Injector
- Callbacks
- Monitor/Checker
- Report Generator

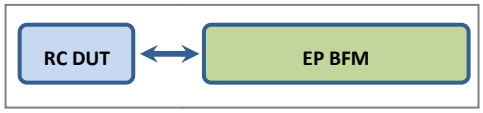

Fig. 1: Simple RC/EP Design

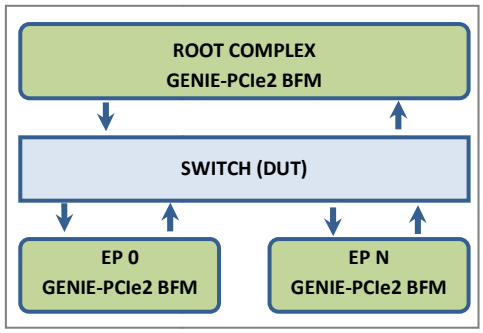

Fig. 2: PCIe Switch Design

FEATURES

❖ Compliant with PCI Express Specification v2.0, v1.1 and 1.0a	❖ Link width support: x1, x2, x4, x8, x12, x16, x32
❖ Supports Gen 1, 2, 8b/10b encoding	❖ Full LTSSM (Link Training & Status) support
❖ Supports up to 8 virtual channels	❖ Full Requester and Completer functions
❖ Verification at PIPE (8 /16/32 bit), 10b, and serial interface	❖ Complete Configurable Order Management logic
❖ Configurable TS1, TS2, SKP Ordered set generation	❖ Automatic /user configurable handling of all layer packets
❖ Supports randomization for packet fields and data payload with or without error injection	❖ Automatic /user configurable generation of flow control packets and credit management
❖ Robust BFM API automates sending TLPs/DLLPs and controlling automatic BFM device response behaviour and link and device state transitions	❖ Supports transaction-oriented request-completion and error injection sequences based on address and command type attributes
❖ Full DL state machines and configurable ACK/NACK and Replay timers	❖ Checks all TLPs for correct formation of headers, prefixes and ECRC
❖ Provides read and write transfers to memory, I/O, and configuration space	❖ Generates block read and write transfers to memory space and message transfers
❖ Language Interface – SystemVerilog & Verilog	❖ Supports Error Injection at all layers
❖ Comprehensive Compliance Suite – PCI-SIG based checklist	❖ Supports OVM/UVM/VMM methodology
❖ Supports Performance evaluations like bandwidth, utilization, efficiency calculations	

DATASHEET
Rev. 2

PRODUCT DETAILS

Single-Link Operation

In the single-link mode, the BFM is configured as a single link supporting x1, x2, x4, x8, x12, x16 or x32 operation. The BFM is enriched with Knobs to provide complete configurability over packet transmission and reception behaviour. Simple and easy APIs allow users to inject packets/errors at any layer level.

RC and EP Operation

As RC or EP the BFM can generate Memory Messages, IO, and Config as requester or completer. In RC mode, the BFM is able to generate I/O and config requests. It can be configured as a loopback master. In EP mode, the BFM supports automatic responses to all transaction types.

PCIe Interface Inspector

The Interface Inspector tracks the traffic of the link and provides protocol-checking capability. Checks are configurable. They can be enabled and disabled individually for a particular test. It generates LOG file and displays protocol specific and transaction information. The log file can be tailored by the user depending on the requirement. Various verbosity levels are supported for warning, debug, errors and log.

The Genie-PCIe Interface Inspector checker provides protocol-checking capability with the following built-in rules:

- Endpoint rules
- Root Complex Integrated Endpoint Rules
- TLPs with Data Payloads Rules
- Routing and Addressing Rules
- First/Last DW Byte Enables Rules
- Memory, I/O & Configuration Request Rules
- Message Request Rules
- Completion Rules
- Request Handling Rules
- Completion Handling Rules
- Transaction Ordering Rules

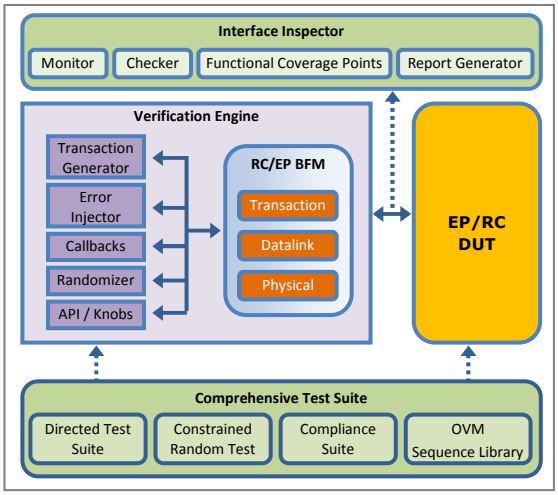

Fig. 3: PCIe 2 Verification Environment

BENEFITS

- ❖ Guarantees compliance to PCIe 2.0 specification
- ❖ Block level and System level verification
- ❖ Reduces overall design and verification costs
- ❖ Reduces test development effort
- ❖ Shortens verification schedule
- ❖ Plug-and-play into all major simulation environments

SUPPORTED SIMULATORS: ALDEC CADENCE MENTOR SYNOPSYS

PCIe 2.0 COMPLIANCE SUITE

Developed by PerfectVIPs, the compliance suite is a PCI-SIG based compliance test with additional compliance coverage from checklists.

- Verifies all layers of PCIe designs
- Provides comprehensive design coverage targeted at Phy, Datalink, Transaction & Configuration Space
- Identifies all protocol violations
- Provides detailed reports on functional coverage
- Provides directed and constrained random regression testing capability
- Developed with actual customer designs

PCIe 2.0 SOLUTIONS

Developed by PerfectVIPs to address different system level PCIe architectures, the following PCIe solutions are available:

Verification IP:
- PCIe 2.0 Root Complex (RC) VIP
- PCIe 2.0 End Point (EP) VIP
- PCIe 2.0 RC/EP VIP (configurable)
- PCIe 2.0 RC Interface Inspector
- PCIe 2.0 EP Interface Inspector

Compliance Suites:
- RC Compliance Test Suite
- EP Compliance Test Suite

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